



e-ISSN: 2319-8753 | p-ISSN: 2320-6710

IJRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 9, Issue 10, October 2020

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 7.512



9940 572 462



6381 907 438



ijirset@gmail.com



www.ijirset.com

Seven Level Inverter with Reduced Number of Switches

Reeba Stephen¹

Lecturer, Department of Electrical and Electronics Engineering, SCMS College of Polytechnics, Perumbavoor, Ernakulam, India¹

ABSTRACT: A multilevel inverter when compared to normal inverters have several advantages. The THD, ripples, and the harmonics will be low. This advantage makes this type of inverters more suitable for normal applications.

KEYWORDS: multilevel inverter, seven level, switching state, switches, zero voltage state

I. INTRODUCTION

Multilevel inverters are nowadays widely used in areas where inverters dominated [3]. As the number of levels of a multilevel inverter increases the lesser will be the harmonics and hence THD will be minimum. Sine wave is the ideal case and as the level of inverter increases more the output becomes similar to sine wave. The conventional multilevel inverter topologies are Diode clamped topology, Flying Capacitor topology, cascaded H bridge topology. The conventional inverter topologies have many disadvantages such as large number of components which makes it bulkier, cost high as the number of components increases etc. Because of this a lot of other topologies have been implemented in order to rectify these errors. In this Multilevel inverter described in this paper the number of components or switches are very less and the THD is very less. As a result the cost for design of this inverter will be very less.

II. CONVENTIONAL METHODS

A. Diode Clamped topology or Neutral clamped topology

In this topology the diodes drag the output voltage to the desired level and hence the name. Advantages are the voltage across the switches are only half of that of dc link voltage. Also diodes are cheaper. The disadvantage of this type of topology is that it requires high speed clamping diodes that must be able to carry full load current and are subjected to severe reverse recovery stress [1]. Although measures to alleviate this problem can be applied and hence this can be a serious condition.

B. Flying Capacitor Topology

In Flying Capacitor Topology we obtain different voltage levels with the help of capacitors [1].

C. Cascaded H Bridge Topology

In this topology H bridges which is a combination of 4 switches plus a DC source is used to obtain any of the two levels of the inverter. This makes the system bulkier and costlier [4].

III. SEVEN LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

In this paper the discussion is about seven level inverter using seven switches [2]. The system is shown in the figure below.

A. Circuit Description

Here we use three voltage sources of 100V each so that we can have an output voltage of maximum value 300V. Here we have seven switches namely S1, S2, S3, ..., S7. The load used is resistive in nature.

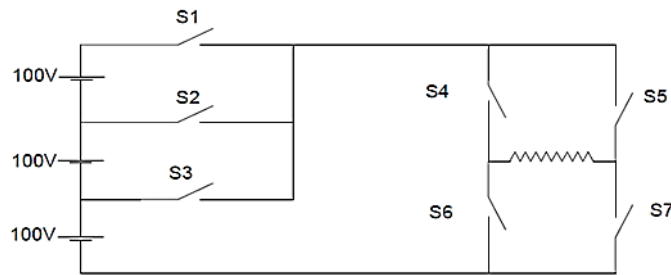


Fig.1: Circuit diagram of seven level inverter with reduced number of switches

B. Working

- When switches S4 and S7 are on the output voltage will be positive
- When switches S5 and S6 are on the output will be negative
- When S1 is on input voltage available is 300V
- When S2 is on input voltage available is 200V
- When S3 is on input voltage available is 100V
- Thus the seven output levels are 0,100,200,300,-100,-200,-300

C. Switching Table

The switching table corresponding to different switches is shown in the table below.

SWITCH	ON TIME POSITIVE HALF CYCLE	ON TIME NEGATIVE HALF CYCLE
S1	3.75ms to 6.25ms	13.75ms TO 16.75ms
S2	2.5ms to 3.75ms,6.25 to 7.5ms	12.5ms to 13.75ms,16.25 to 17.5ms
S3	1.25ms to 2.5ms,7.5ms to 8.75ms	11.25ms to 12.5ms,17.5ms to 18.75ms
S4,S7	0-10ms	X
S5,S6	X	10-20ms

TABLE:1 Switching Table

IV.SIMULATION AND RESULTS

The simulation is done in MATLAB/SIMULINK. The switches used are IGBT's. The switching table is shown in the above section

A. Simulation Diagram

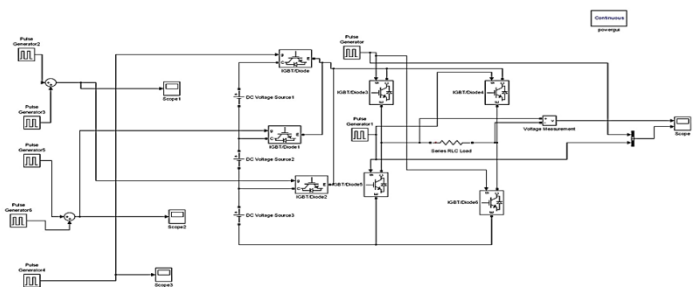


Fig.2: Simulation of seven level inverter with reduced number of switches

IV. EXPERIMENTAL RESULTS

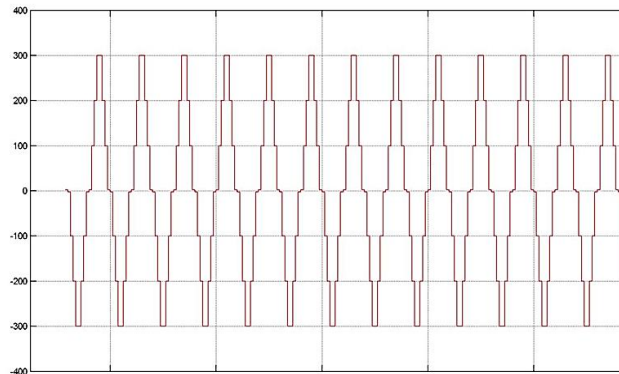


Fig.3: Output from MATLAB simulation

The net output of the implemented circuit is shown in the diagram above. The output levels of 100,200,300,0,-100,-200,-300V is obtained.

V. CONCLUSION

The topology used in this paper has a lot of advantages compared to conventional methods and also the number of switches used is less. This can reduce the cost of the system.

REFERENCES

- [1] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies modulation techniques and applications", *Renew. Sustain. Energy Rev.*, vol. 76, pp. 1248-1282, Sep. 2017
- [2] Jacob James Nedumgatt, Vijayakumar D, A. Kirubakaran, Umashankar S" A multilevel inverter with reduced number of switches",2012 IEEE Students Conference on Electrical and Electronics and Computer Science.
- [3] S. Kouro et al., "Recent advances and industrial applications of multilevel converters", *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.
- [4] EbrahimBabaei" A cascade Multilevel converter Topology with reduced number of switches"IEEE Transactions On Power Electronics vol.23,no.6 November 2008.



INNO  **SPACE**
SJIF Scientific Journal Impact Factor

**Impact Factor:
7.512**

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 **9940 572 462**  **6381 907 438**  **ijirset@gmail.com**



www.ijirset.com

Scan to save the contact details